

# CBT3257A

## Quad 1-of-2 multiplexer/demultiplexer

Rev. 02 — 4 July 2007

Product data sheet

### 1. General description

The CBT3257A is a quad 1-of-2 high-speed TTL-compatible multiplexer/demultiplexer. The low ON-state resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

Output enable ( $\overline{OE}$ ) and select-control (S) inputs select the appropriate nB1 and nB2 outputs for the nA input data.

The CBT3257A is characterized for operation from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

### 2. Features

- $5\ \Omega$  switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA

### 3. Ordering information

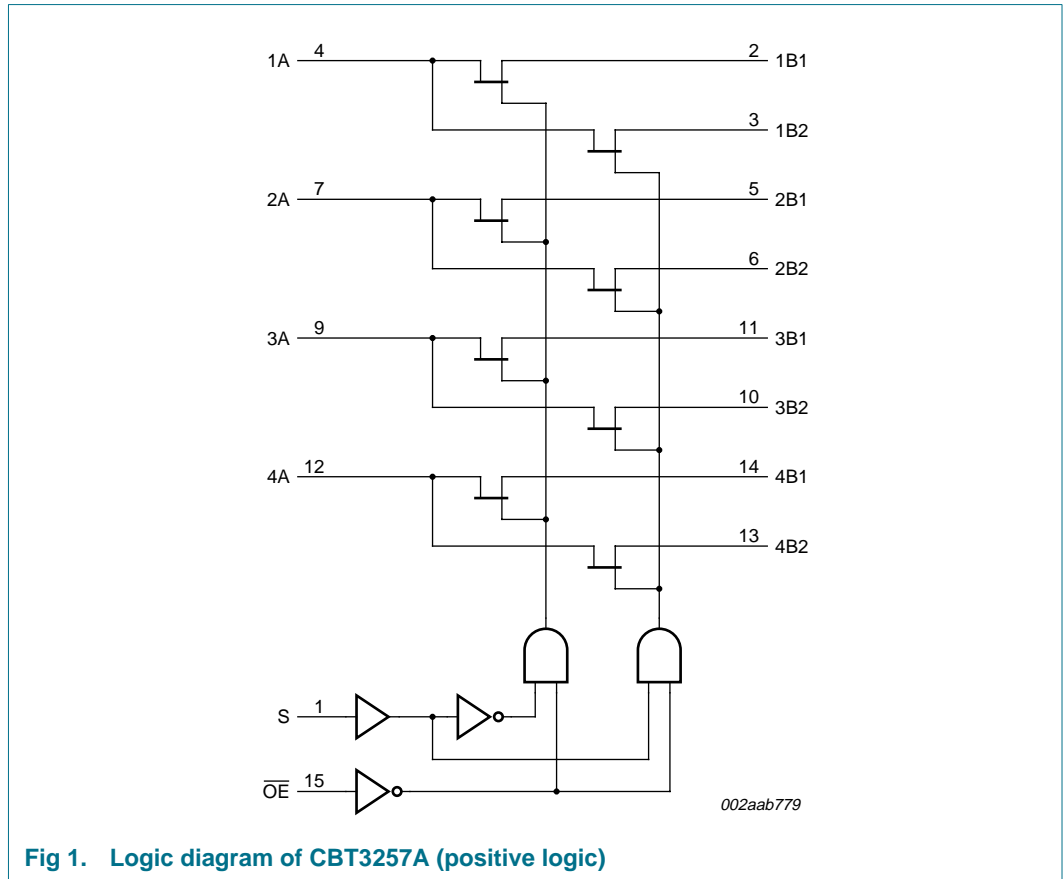
**Table 1. Ordering information**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Topside mark	Package		
		Name	Description	Version
CBT3257AD	CBT3257AD	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3257ADB	3257A	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
CBT3257ADS	CT3257A	SSOP16 <sup>[1]</sup>	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
CBT3257APW	CT3257A	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

[1] Also known as QSOP16.

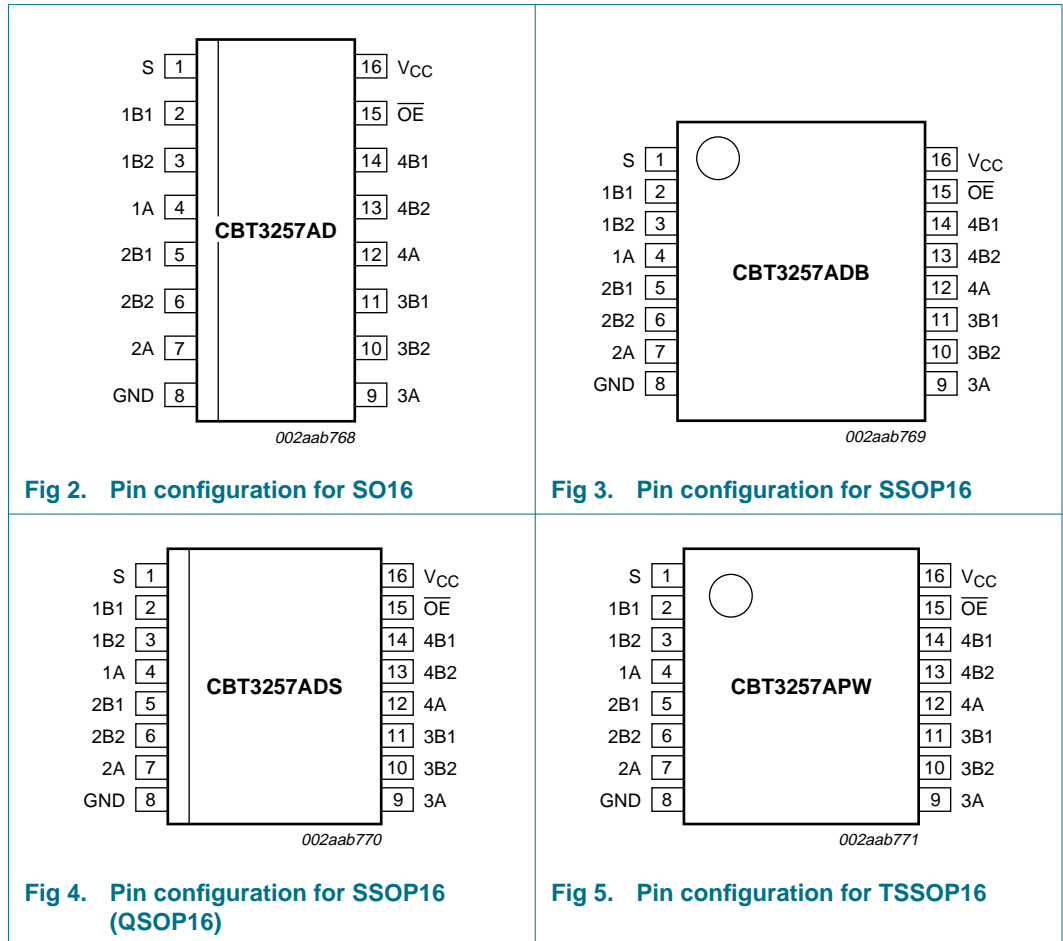
**4. Functional diagram**



**Fig 1. Logic diagram of CBT3257A (positive logic)**

**5. Pinning information**

**5.1 Pinning**



**Fig 2. Pin configuration for SO16**

**Fig 3. Pin configuration for SSOP16**

**Fig 4. Pin configuration for SSOP16 (QSOP16)**

**Fig 5. Pin configuration for TSSOP16**

**5.2 Pin description**

**Table 2. Pin description**

Symbol	Pin	Description
S	1	select control input
1B1, 1B2, 2B1, 2B2, 3B1, 3B2, 4B1, 4B2	2, 3, 5, 6, 10, 11, 13, 14	B outputs <sup>[1]</sup>
1A, 2A, 3A, 4A	4, 7, 9, 12	A inputs
GND	8	ground (0 V)
OE	15	output enable (active LOW)
V <sub>CC</sub>	16	positive supply voltage

[1] B outputs are inputs if A inputs are outputs.

## 6. Functional description

Refer to [Figure 1 “Logic diagram of CBT3257A \(positive logic\)”](#).

### 6.1 Function table

**Table 3. Function selection**

*H = HIGH voltage level; L = LOW voltage level; X = Don't care.*

Inputs		Function
OE	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	disconnect

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		[1] -0.5	+7.0	V
$I_{CCC}$	continuous current through each $V_{CC}$ or GND pin		-	128	mA
$I_{IK}$	input clamping current	$V_I < 0\text{ V}$	-	-50	mA
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

*All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$T_{amb}$	ambient temperature	operating in free-air	-40	-	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}$ ; $I_I = -18\text{ mA}$	-	-	-1.2	V
$V_{pass}$	pass voltage	$V_I = V_{CC} = 5.0\text{ V}$ ; $I_O = -100\text{ }\mu\text{A}$	3.4	3.6	3.9	V
$I_{LI}$	input leakage current	$V_{CC} = 5.5\text{ V}$ ; $V_I = \text{GND}$ or $5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}$ ; $I_O = 0\text{ mA}$ ; $V_I = V_{CC}$ or $\text{GND}$	-	-	3	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input; $V_{CC} = 5.5\text{ V}$ ; one input at $3.4\text{ V}$ , other inputs at $V_{CC}$ or $\text{GND}$	<sup>[2]</sup> -	-	2.5	mA
$C_I$	input capacitance	control pins; $V_I = 3\text{ V}$ or $0\text{ V}$	-	3.3	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; $V_O = 3\text{ V}$ or $0\text{ V}$ ; $\overline{\text{OE}} = V_{CC}$	-	9.9	-	pF
		B port; $V_O = 3\text{ V}$ or $0\text{ V}$ ; $\overline{\text{OE}} = V_{CC}$	-	6.4	-	pF
$R_{on}$	ON-state resistance	$V_{CC} = 4.5\text{ V}$	<sup>[3]</sup> -	-	-	-
		$V_I = 0\text{ V}$ ; $I_I = 64\text{ mA}$	-	5	7	$\Omega$
		$V_I = 0\text{ V}$ ; $I_I = 30\text{ mA}$	-	5	7	$\Omega$
		$V_I = 2.4\text{ V}$ ; $I_I = 15\text{ mA}$	-	10	15	$\Omega$

[1] All typical values are measured at  $V_{CC} = 5\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or  $\text{GND}$ .

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (A or B) terminals.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$ ;  $C_L = 50\text{ pF}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{pd}$	propagation delay	from nA input to nBn output, or from nBn input to nA output	<sup>[1]</sup> -	-	0.25	ns
		from S input to nA output	<sup>[1]</sup> 1.6	-	5.0	ns
$t_{en}$	enable time	from $\overline{\text{OE}}$ input to nA or nBn output	<sup>[2]</sup> 1.8	-	5.1	ns
		from S input to nBn output	<sup>[2]</sup> 1.6	-	5.2	ns
$t_{dis}$	disable time	from $\overline{\text{OE}}$ input to nA or nBn output	<sup>[3]</sup> 2.2	-	5.5	ns
		from S input to nBn output	<sup>[3]</sup> 1.0	-	5.0	ns

[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON-state resistance of the switch and a load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] Output enable time to HIGH and LOW level.

[3] Output disable time from HIGH and LOW level.

10.1 AC waveforms

$V_I = \text{GND to } 3.0 \text{ V.}$

$t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

$t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

$t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

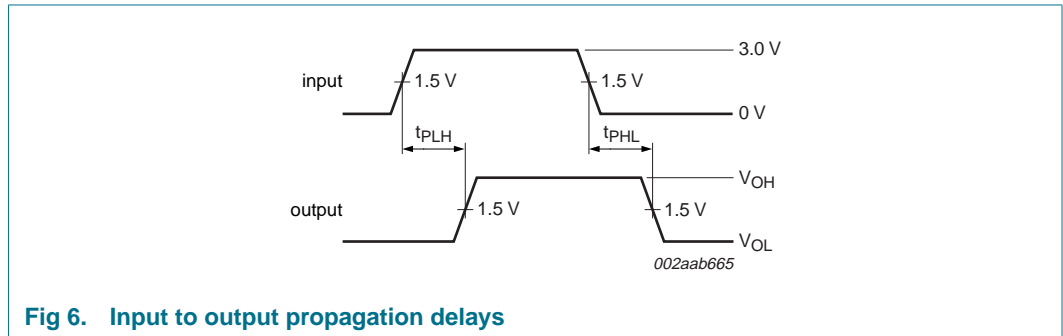
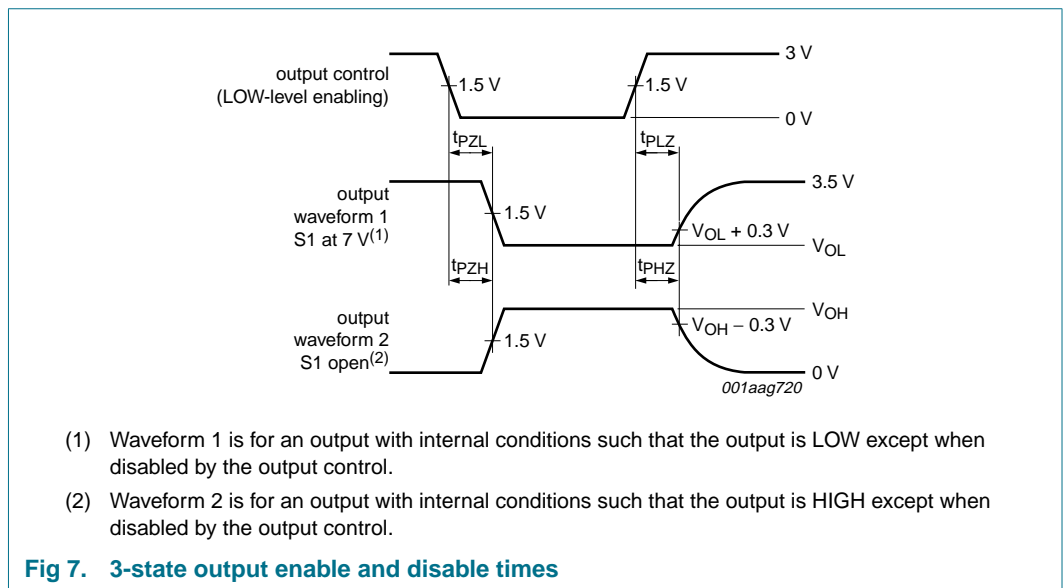


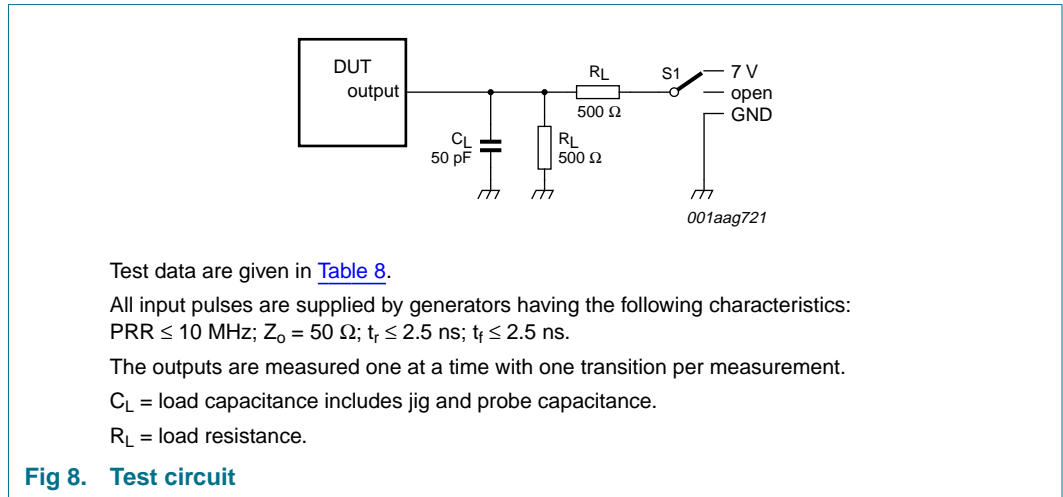
Fig 6. Input to output propagation delays



- (1) Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
- (2) Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Fig 7. 3-state output enable and disable times

### 11. Test information



**Table 8. Test data**

Test	Load		Switch
	$C_L$	$R_L$	
$t_{pd}$	50 pF	500 $\Omega$	open
$t_{PLZ}, t_{PZL}$	50 pF	500 $\Omega$	7 V
$t_{PHZ}, t_{PZH}$	50 pF	500 $\Omega$	open

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

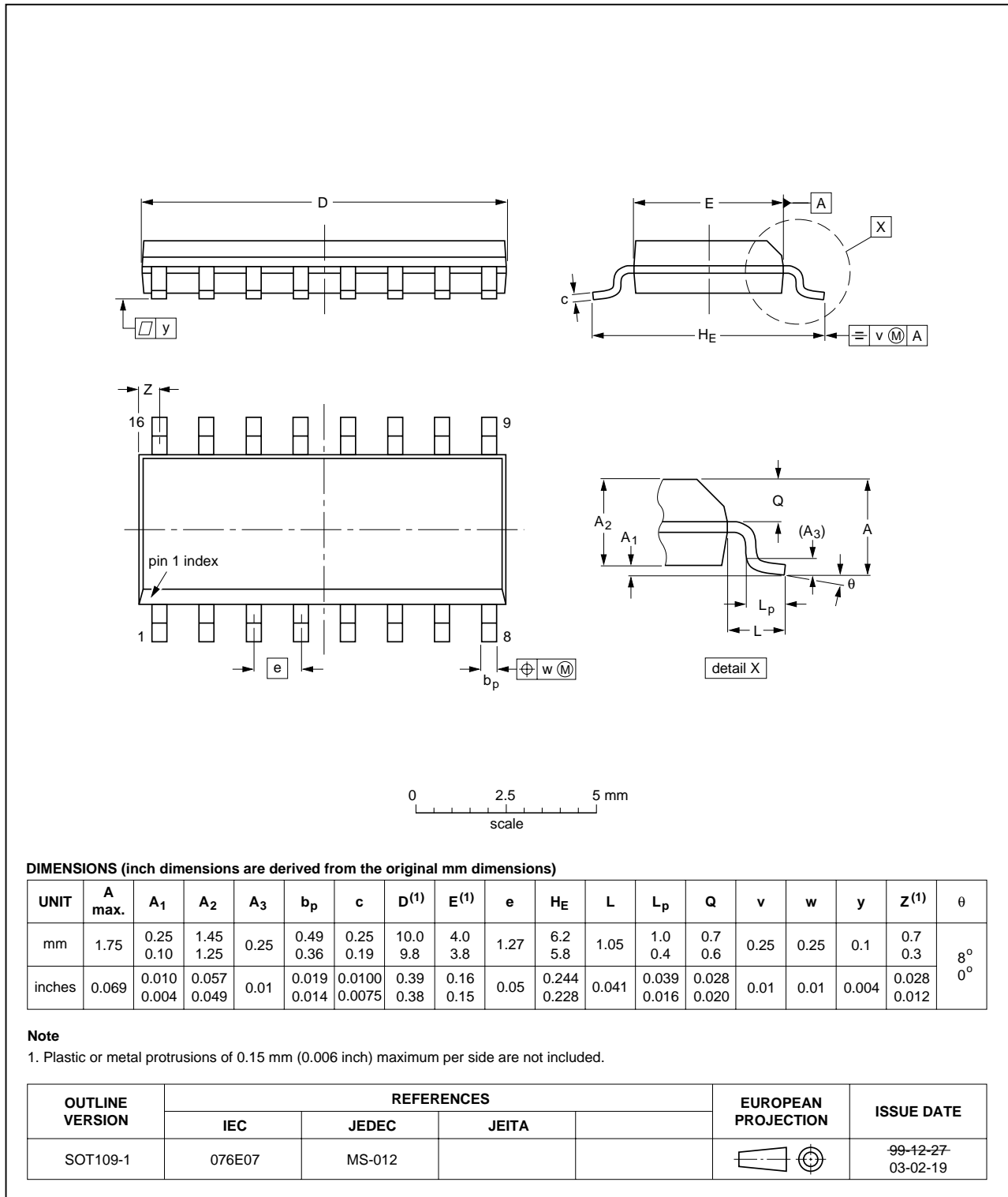


Fig 9. Package outline SOT109-1 (SO16)



SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

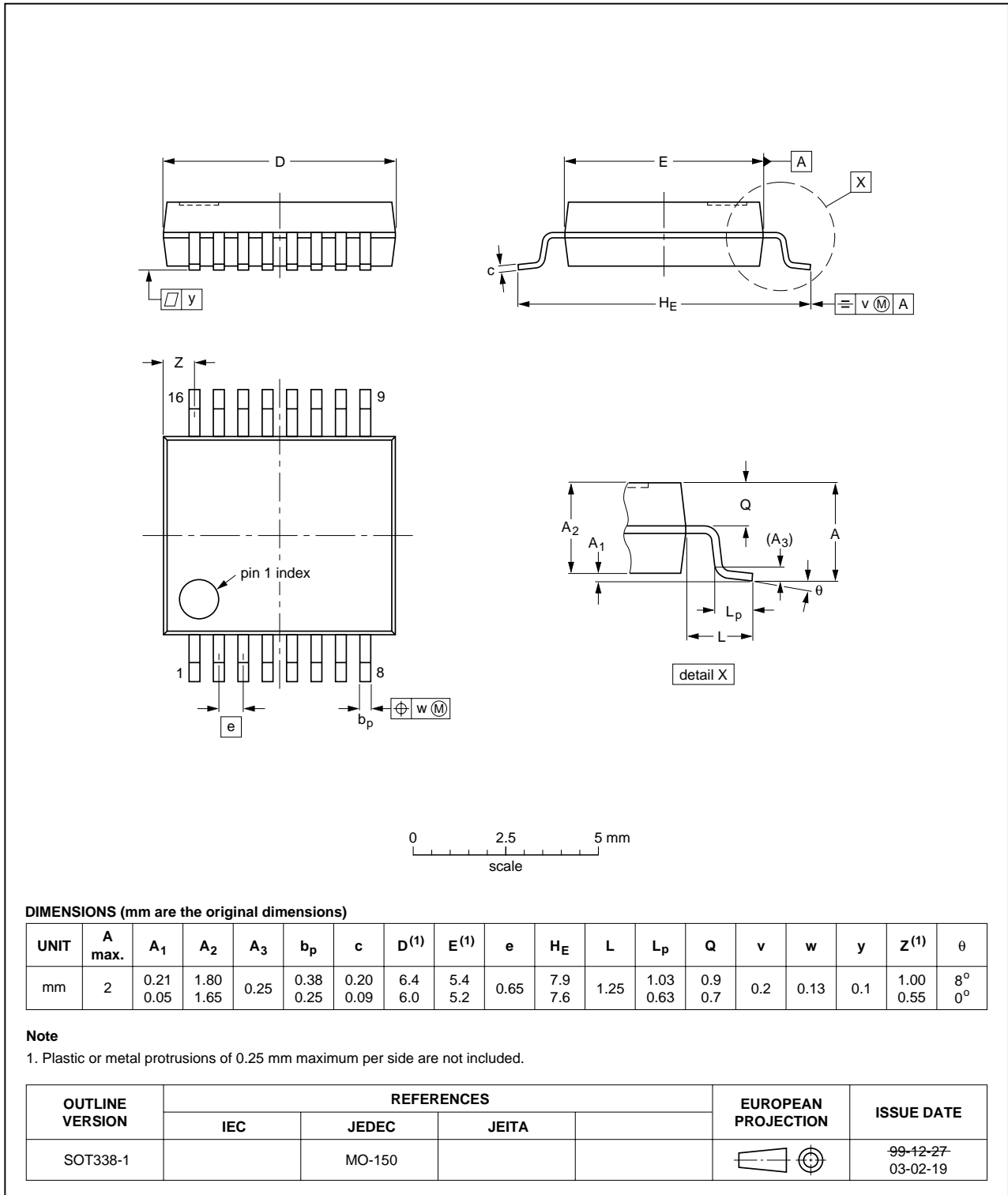


Fig 10. Package outline SOT338-1 (SSOP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

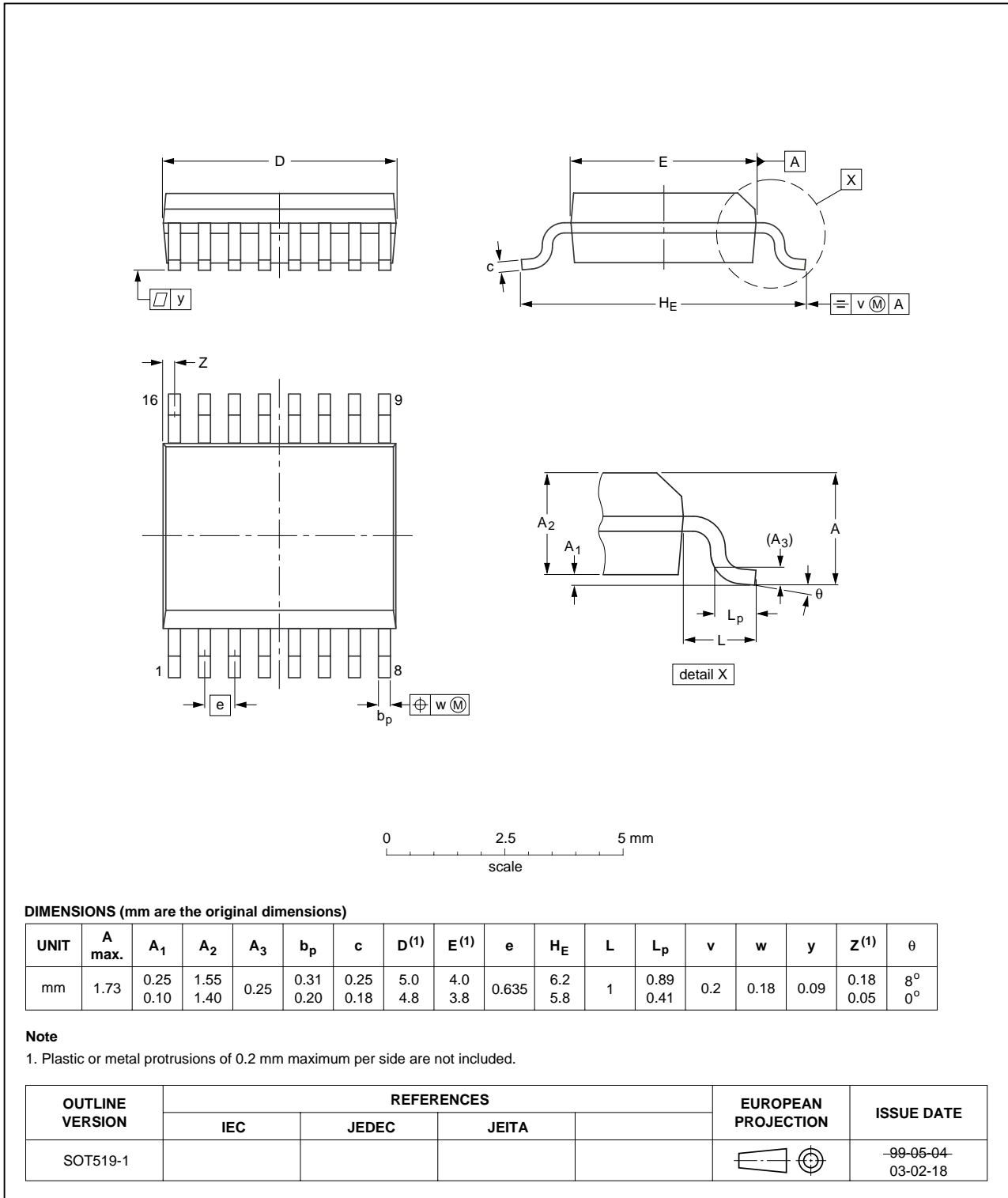


Fig 11. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

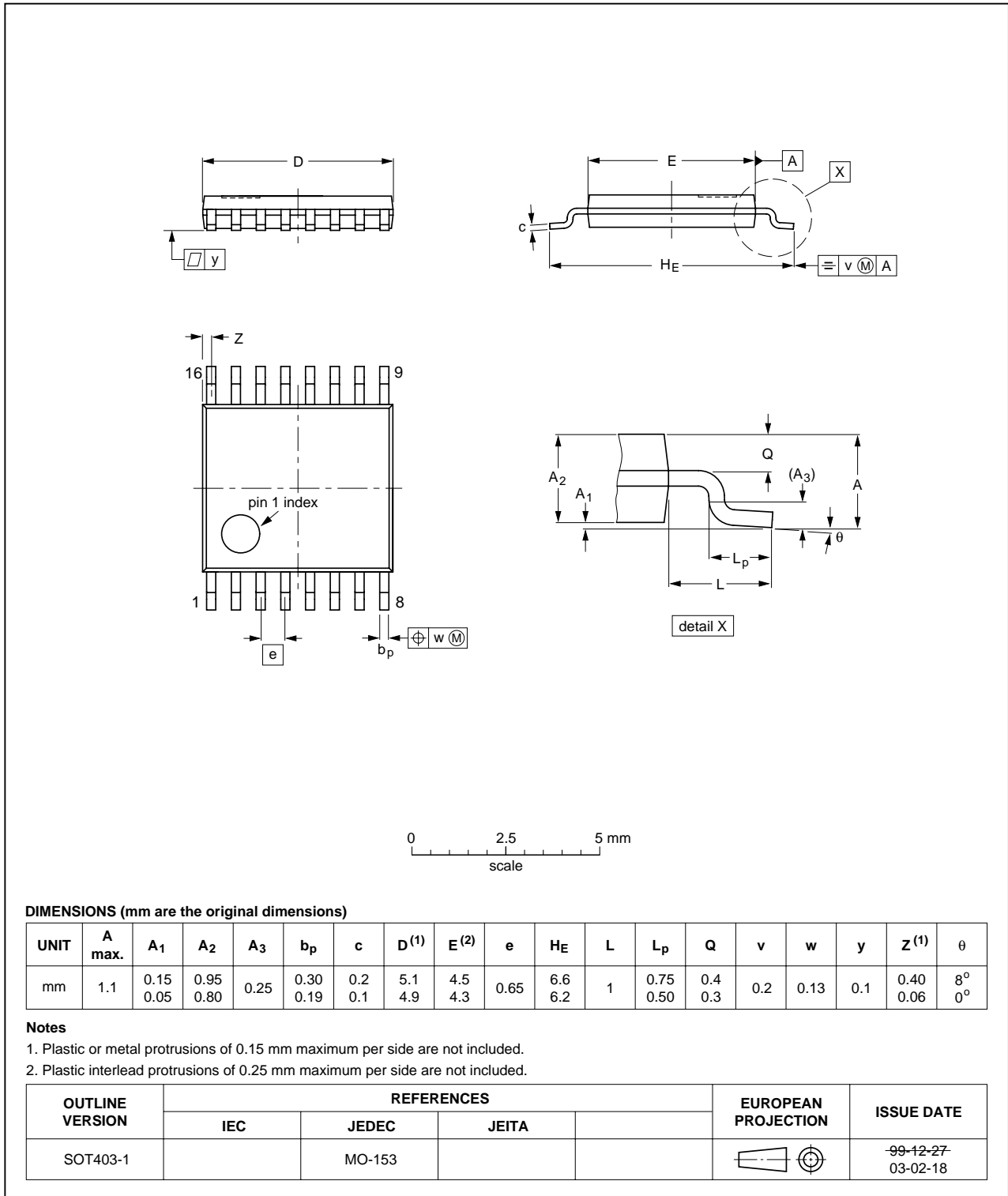


Fig 12. Package outline SOT403-1 (TSSOP16)

## 13. Abbreviations

**Table 9. Abbreviations**

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3257A_2	20070704	Product data sheet	-	CBT3257A_1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Table 1</a>: Topside marking changed for versions SOT338-1 and SOT403-1.</li> <li>• Soldering information removed.</li> </ul>			
CBT3257A_1	20051027	Product data sheet	-	-

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### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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